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Docket No.: DATUMTE.018A

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APPEAL BRIEF

Appellants	:	Plasterer, et al.
App. No	:	10/820,381
Filed	:	April 8, 2004
For	:	SYSTEMS AND METHODS FOR ACTIVELY PEAKED CURRENT-MODE LOGIC
Examiner	:	Anh Q. Tran
Art Unit	:	2819

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In accordance with the Notice of Appeal filed June 20, 2006, Appellants submit this Appeal Brief.

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I. REAL PARTY IN INTEREST

The real party of interest in the present application is PMC-Sierra, Inc.

II. RELATED APPEALS AND INTERFERENCES

No related appeals, interferences or judicial proceedings are currently pending.

III. STATUS OF CLAIMS

Claims 1-4 and 42-48 are currently pending and rejected. Claims 5-41 are withdrawn. Claims 1-4 and 42-48 are attached hereto as an appendix. All of the pending claims were finally rejected by the Examiner and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No claims have been amended subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to circuits, and more particularly, to relatively-high speed differential logic circuits. Each independent claim is summarized below, with citations to corresponding portions of the specification and drawings as required by 37 C.F.R. § 41.37(c)(1)(v). These citations are provided in order to illustrate specific examples and embodiments of the recited claim language, and are not intended to limit the claims.

Independent Claim 1 is directed to a circuit (800) having a differential circuit (804, 806), a first current source (802), a first active load (808), and a second active load (810) (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]), which form at least part of a state machine (3000) (Figure 30, page 34, line 24 to page 35, line 7, paragraphs [0161] to [0162], page 10, lines 15-17, paragraph [0037]). The first active load (808) has an inductive impedance characteristic as seen from the drain of the first NMOS transistor (804, 806) (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]). The second active load (810) has an inductive impedance characteristic as seen from the drain of the second NMOS transistor (806) (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]).

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Independent Claim 42 is directed to an integrated circuit having a differential logic circuit (804, 806) and active loads (808, 810) (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]), which form at least part of a state machine (3000) (Figure 30, page 34, line 24 to page 35, line 7, paragraphs [0161] to [0162], page 10, lines 15-17, paragraph [0037]). The differential logic circuit (804, 806) is implemented with current-controlled complementary metal-oxide semiconductor field-effect transistor circuits (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]). The active loads (808, 810) mimic the response of inductors without inclusion of an explicit inductor (Figure 8, page 20, line 2 to page 21, line 19, paragraphs [0093] to [0100]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds for rejection are to be reviewed on appeal:

A) The rejection of independent Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,788,103 to Feldman, et al. ("Feldman"), in view of U.S. Patent Application Publication No. 2004/0088594 by Canagasaby, et al. ("Canagasaby").

B) The rejection of independent Claim 42 under 35 U.S.C. § 103(a) as being unpatentable over Feldman in view of Canagasaby.

VII. ARGUMENT

Discussion of the Canagasaby reference relied upon by the Examiner.

Canagasaby teaches that the "receiver tracking mechanism 330" (paragraph [0040]), the "receiver tracking mechanism, as shown in FIG. 9," and the "drift direction predictor, as shown in FIG. 9" (paragraph [0121]), may be a state machine. Active loads are not described in connection with the state machines of Canagasaby.

Active loads 1510-1512 are illustrated in Figure 15, which illustrates "the example phase tracking interpolator 340" (paragraph [0067]). Canagasaby does not teach or suggest that the interpolator 340 is a state machine.

Therefore, there is no state machine in Canagasaby that has an active load.

(A) Claim 1 is not obvious in view of Feldman and Canagasaby

The Examiner acknowledges that Feldman does not teach or suggest "wherein the differential circuit, the first current source, the first active load, and the second active load form at least part of a state machine." The Examiner uses Canagasaby to provide the missing element.

In the Final Office Action, the Examiner asserts that:

> Canagasaby shows a state machine (330 and 340 in Fig. 3 are considered as a state machine, [0040] in a micro-processor shows as chip A or B in figures 1A-1B) comprises a differential circuit (Figure 15) having a current source (1540A-D), the first active load (1510, active load [0070]), and the second active load (1512).

In the Advisory Action, Examiner asserts that:

> 330 and 340 in figure 3 are part of a microprocessor that is capable of performing state function or control function, furthermore, it is well known that logic gates and latches are use to form larger and more complex circuit."

As illustrated in Figure 3, the receiver tracking mechanism 330 and the interpolator 340 are distinct blocks. The Examiner combines the active load properties of the interpolator 340 with the state machine attributes of the receiver tracking mechanism 330 by considering both together as "a state machine." Canagasaby teaches that the "receiver tracking mechanism 330 may be implemented as a state machine" (page 3, lines 37-38, paragraph [0040]), but does not teach or suggest that the interpolator 340 is a state machine. Accordingly, the Examiner's characterization of Canagasby is an unsupported modification of Canagasaby, and thus, Canagasaby does not provide the missing element.

Therefore, Feldman and Canagasaby fail to teach all the claim limitations as required by 35 U.S.C. § 103(a). In order to establish *prima facie* obviousness of a claimed invention under 35 U.S.C. § 103(a), all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

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(B) Claim 42 is not obvious in view of Feldman and Canagasaby

The Examiner acknowledges that Feldman does not teach or suggest "the differential circuit and the active load form at least part of a state machine." The Examiner uses Canagasaby to provide the missing element.

In the Final Office Action, the Examiner asserts that "Canagasaby shows a state machine (330 and 340 in Fig. 3 are considered as a state machine...)." By considering blocks 330 and 340 of Canagasaby together as a state machine, the Examiner combines the active load properties of the interpolator 340 with the state machine attributes of the receive tracking mechanism 330. This appears to be an unsupportable modification of Canagasaby. Accordingly, Canagasaby does not provide the missing element.

Therefore, Feldman and Canagasaby fail to teach all the claim limitations as required by 35 U.S.C. § 103(a). In order to establish *prima facie* obviousness of a claimed invention under 35 U.S.C. § 103(a), all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

VIII. CONCLUSION

For the reasons set forth above, Appellants respectfully submit that the rejections of Claims 1 and 42 are improper, and request that these rejections be reversed.

Respectfully submitted,

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Dated: August 31, 2006

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CLAIMS APPENDIX

1. A circuit fabricated in an integrated circuit with a differential input and a differential output, the circuit comprising:

a differential circuit with a first NMOS transistor and a second NMOS transistor, where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled, where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive the differential input, and where the drain of the first NMOS transistor and the drain of the second NMOS transistor are configured to provide the differential output;

a first current source with at least a first terminal, where the first terminal of the first current source is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor;

a first active load with at least a first terminal coupled to the drain of the first NMOS transistor of the differential circuit, where the first terminal of the first active load has an inductive impedance characteristic as seen from the drain of the first NMOS transistor; and

a second active load coupled to the drain of the second NMOS transistor of the differential circuit, where the second active load has an inductive impedance characteristic as seen from the drain of the second NMOS transistor;

wherein the differential circuit, the first current source, the first active load, and the second active load form at least part of a state machine.

2. The circuit as defined in Claim 1, where the first current source is an NMOS transistor with a source, a gate, and a drain, and where the first terminal of the first current source corresponds to the drain of the NMOS transistor.

3. The circuit as defined in Claim 1, wherein the first active load and the second active load exhibit the inductive impedance characteristic without benefit of a passive inductor.

4. The circuit as defined in Claim 1, wherein the first active load further comprises:

a third NMOS transistor with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference; and

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the third NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference.

42. An integrated circuit with metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated on a silicon substrate, the integrated circuit comprising:

a differential logic circuit implemented with current-controlled complementary metal-oxide semiconductor field-effect transistor circuits; and

active loads coupled to the transistor circuits of the differential logic circuit, where the active loads mimic the response of inductors without inclusion of an explicit inductor;

wherein the differential logic circuit and the active loads form at least part of a state machine.

43. The integrated circuit as defined in Claim 42, wherein the differential logic circuit is configured to correspond to at least a portion of a buffer, an inverter, an AND gate, a NAND gate, an OR gate, a NOR gate, a multiplexer, a latch, or a flip-flop.

44. The integrated circuit as defined in Claim 42, wherein the state machine is embodied in a microprocessor.

45. The integrated circuit as defined in Claim 42, wherein the state machine is embodied in a graphics processor.

46. The integrated circuit as defined in Claim 42, wherein the state machine is embodied in a serial-deserializer (SERDES).

47. The integrated circuit as defined in Claim 42, wherein the state machine comprises at least a combination of logic cells and a flip-flop.

48. The circuit as defined in Claim 1, wherein the state machine comprises at least a combination of logic cells and a flip-flop.

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EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

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